RELIABILITY REPORT

FOR

MAX6023EBTxx

CHIP SCALE DEVICES

July 17, 2003

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.

SUNNYVALE, CA 94086

Written by

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Conclusion

The MAX6023 successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I. Device Description

A. General

The MAX6023 is a family of low-dropout, micropower voltage references in a 5-bump, chip-scale package (UCSP™). The MAX6023 series-mode (three-terminal) references, which operate with input voltages from 2.5V to 12.6V (1.25V and 2.048V options) or (V_{OUT} + 0.2V) to 12.6V (all other voltage options), are available with output voltage options of 1.25V, 2.048V, 2.5V, 3.0V, 4.096V, 4.5V, and 5.0V. These devices are guaranteed an initial accuracy of ±0.2% and 30ppm/°C temperature drift over the -40°C to +85°C extended temperature range.

UCSPs offer the benefit of moving to smaller footprint and lower profile devices, significantly smaller than even SC70 or SOT23 plastic surface-mount packages. The significantly lower profile (compared to plastic SMD packages) of the UCSP makes the device ideal for height-critical applications. Miniature UCSP packages also enable device placement close to sources and allow more flexibility in a complex or large design layout.

The MAX6023 voltage references use only 27µA of supply current. And unlike shunt-mode (two-terminal) references, the supply current of the MAX6023 family varies only 0.8µA/V with supply-voltage changes, translating to longer battery life. Additionally, these internally compensated devices do not require an external compensation capacitor and are stable up to 2.2nF of load capacitance. The low-dropout voltage and the low supply current make these devices ideal for battery-operated systems.

B. Absolute Maximum Ratings

Item	Rating
(Voltages Referenced to GND)	
IN	-0.3V to +13.5V
OUT	-0.3V to (VIN + 0.3V)
Output Short Circuit to GND or IN (VIN < 6V)	Continuous
Output Short Circuit to GND or IN (VIN = 6V)	60s
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Bump Temperature (soldering, 10s)	+300°C
Continuous Power Dissipation	
5-Bump UCSP	273mW
Derates above +70°C	
5-Bump UCSP	2.4mW/°C

Note 1: This device is constructed using a unique set of packaging techniques that impose a limit on the thermal profile the device can be exposed to during board-level solder attach and rework. This limit permits only the use of solder profiles recommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and convection reflow. Preheating is required. Hand or wave soldering is not allowed.

II. Manufacturing Information

A. Description/Function:	Precision, Low-Power, Low-Dropout, UCSP Voltage Reference
B. Process:	S12 (Standard 1.2 micron silicon gate CMOS)
C. Number of Device Transistors:	70
D. Fabrication Location:	Oregon, USA
E. Assembly Location:	Philippines or USA
F. Date of Initial Production:	January, 2001

III. Packaging Information

A. Package Type:	**5-Bump UCSP**
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	N/A
E. Bondwire:	N/A
F. Mold Material:	N/A
G. Assembly Diagram:	# 05-0901-0164
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard JESD22-112:	Level 1

IV. Die Information

A. Dimensions:	63 x 43 mils
B. Passivation:	SiN/SiO (nitride/oxide)
C. Interconnect:	Aluminum/Si (Si = 1%)
D. Backside Metallization:	None
E. Minimum Metal Width:	1.2 microns (as drawn)
F. Minimum Metal Spacing:	1.2 microns (as drawn)
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO_2
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts: Jim Pedicord (Manager, Reliability Operations)
Bryan Preeshl (Executive Director**)**
Kenneth Huening (Vice President)

B. Outgoing Inspection Level: 0.1% for all electrical parameters guaranteed by the Datasheet.
0.1% For all Visual Defects.

C. Observed Outgoing Defect Rate: < 50 ppm

D. Sampling Plan: Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in **Table 1**. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{MTTF} = \frac{1.83}{192 \times 4389 \times 57 \times 2}$$ (Chi square value for MTTF upper limit)

Temperature Acceleration factor assuming an activation energy of 0.8eV

$\lambda = 19.05 \times 10^{-9}$

$\lambda = 19.05$ F.I.T. (60% confidence level @ 25°C)

This low failure rate represents data collected from Maxim's reliability monitor program. In addition to routine production Burn-In, Maxim pulls a sample from every fabrication process three times per week and subjects it to an extended Burn-In prior to shipment to ensure its reliability. The reliability control level for each lot to be shipped as standard product is 59 F.I.T. at a 60% confidence level, which equates to 3 failures in an 80 piece sample. Maxim performs failure analysis on any lot that exceeds this reliability control level. Attached Burn-In Schematic (Spec. # 06-5114) shows the static Burn-In circuit. Maxim also performs quarterly 1000 hour life test monitors. This data is published in the Product Reliability Report (**RR-1M**).

B. Moisture Resistance Tests

Maxim pulls pressure pot samples from every assembly process three times per week. Each lot sample must meet an LTPD = 20 or less before shipment as standard product. Additionally, the industry standard 85°C/85%RH testing is done per generic device/package family once a quarter.

C. E.S.D. and Latch-Up Testing

The RF39 die type has been found to have all pins able to withstand a transient pulse of ±1500V, per Mil-Std-883 Method 3015 (reference attached ESD Test Circuit). Latch-Up testing has shown that this device withstands a current of ±250mA.

Table 1
Reliability Evaluation Test Results

MAX6034EBTxx

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	PACKAGE	SAMPLE SIZE	NUMBER OF FAILURES
Static Life Test (Note 1)					
	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality		77	0
Moisture Testing (Note 2)					
Pressure Pot	Ta = 121°C P = 15 psi. RH= 100% Time = 168hrs.	DC Parameters & functionality	UCSP	77	0
85/85	Ta = 85°C RH = 85% Biased Time = 1000hrs.	DC Parameters & functionality		N/A	N/A
Mechanical Stress (Note 2)					
Temperature Cycle	-40°C/125°C 1000 Cycles Slow Ramp (Note 3)	DC Parameters	QFN UCSP	77 77	0 0

Note 1: Life Test Data may represent plastic DIP qualification lots.
Note 2: Generic Package/Process data
Note 3: UCSP Temperature Cycle performed at with a ramp rate of 11°C/minute, dwell=15 minutes, one cycle/hour

Attachment #1

TABLE II. Pin combination to be tested. 1/ 2/

	Terminal A (Each pin individually connected to terminal A with the other floating)	Terminal B (The common combination of all like-named pins connected to terminal B)
1.	All pins except V_{PS1} 3/	All V_{PS1} pins
2.	All input and output pins	All other input-output pins

1/ Table II is restated in narrative form in 3.4 below.
2/ No connects are not to be tested.
3/ Repeat pin combination I for each named Power supply and for ground

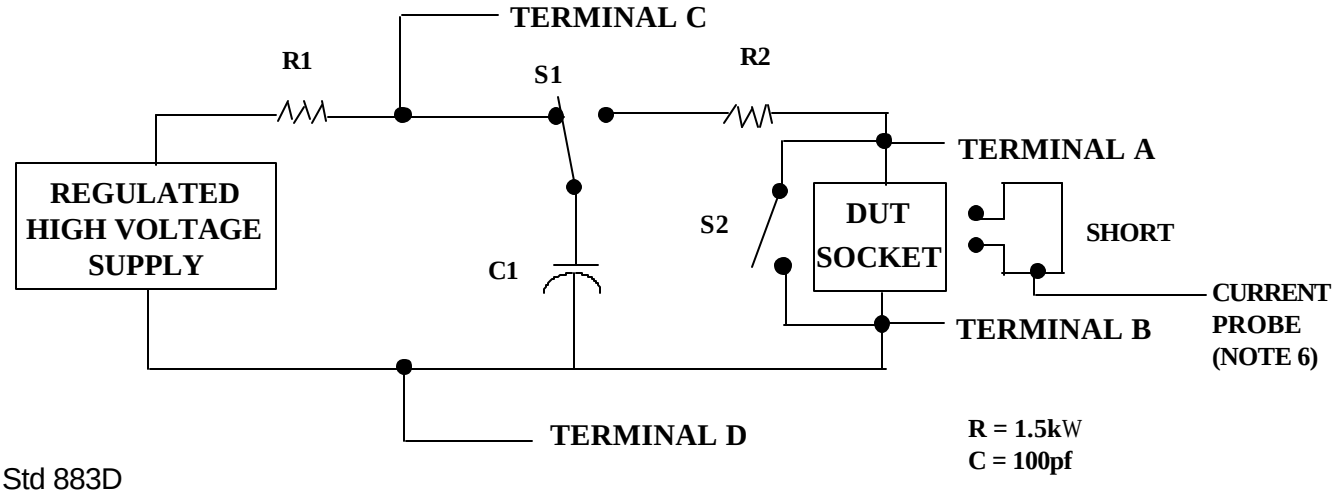
(e.g., where V_{PS1} is V_{DD}, V_{CC}, V_{SS}, V_{BB}, GND, $+V_S$, $-V_S$, V_{REF}, etc).

3.4 Pin combinations to be tested.

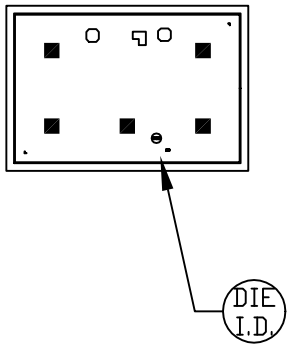
a. Each pin individually connected to terminal A with respect to the device ground pin(s) connected to terminal B. All pins except the one being tested and the ground pin(s) shall be open.

b. Each pin individually connected to terminal A with respect to each different set of a combination of all named power supply pins (e.g., V_{SS1}, or V_{SS2} or V_{SS3} or V_{CC1}, or V_{CC2}) connected to terminal B. All pins except the one being tested and the power supply pin or set of pins shall be open.

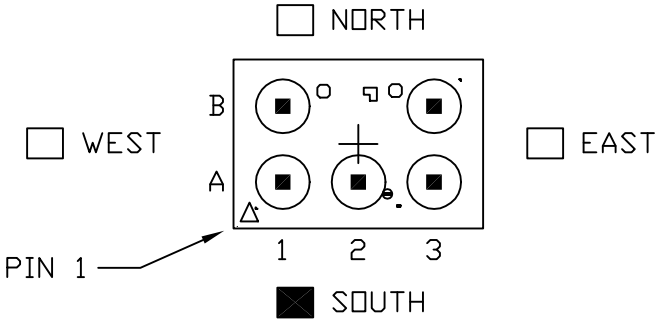
c. Each input and each output individually connected to terminal A with respect to a combination of all the other input and output pins connected to terminal B. All pins except the input or output pin being tested and the combination of all the other input and output pins shall be open.



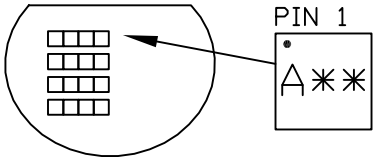
ORIGINAL CHIP



AFTER BUMP



SELECT THE BOX INDICATING THE WAFER FLAT SIDE
WITH RESPECT TO PIN 1.

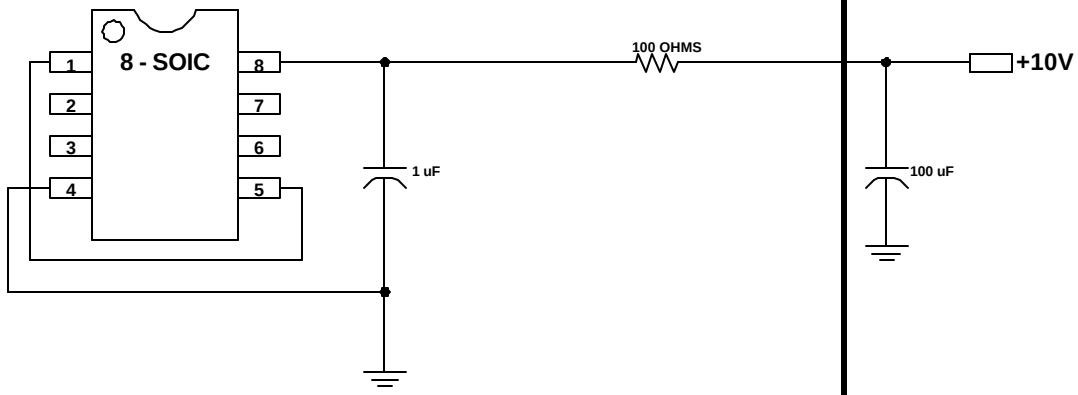


PART MARKING ORIENTATION
IN REFERENCE TO WAFER FLAT
(MARK IS ON WAFER BACKSIDE)

PKG. CODE: B6-4		SIGNATURES	DATE	MAXIM CONFIDENTIAL & PROPRIETARY	
CAV./PAD SIZE: N/A	PKG.			BOND DIAGRAM #: 05-0901-0164	REV: B
	DESIGN				

ONCE PER SOCKET

ONCE PER BOARD



DEVICES: MAX 6023/6012/6021/6025/6041/6045/ 6050/6120/6125/6141/6145/6150/6160/6520
MAX. EXPECTED CURRENT = 60uA

DRAWN BY: HAK TAN

NOTES: